AN10609_2

PN532 application note, C106 appendix

Rev. 1.0 — March 10, 2008 **Application note**

Document information

Info	Content
Keywords	PN532C106, PN532 v1.6, Low Battery mode
Abstract	This document described changes between PN532C104 and PN532C106

Revision history

Rev	Date	Description
1.0	March 10, 2008	First draft of AN10609_2, PN532 application note, C106 appendix. It is based on AN10609_1 rev 1.1

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1. Introduction

This document is a complement to PN532C104 application note, AN10449_1 (file 133910.pdf). The audience must have the two documents, PN532C104 application note and this one, PN532C106 appendix application note.

This document is an appendix to PN532C104 application note. It underlines differences between PN532C104 and PN532C106.

The PN532C106 main differences compared with PN532C104:

- Possible host interface: HSU, I2C or SPI mode 0 (no more SPI mode 1, 2, 3)
- “Low battery” mode

“Low battery” mode is the default mode of PN532C106. It is described page 10.

References

Ref.number	*Document name*	
1	PN532 C106 user manual	UM0701-02
2	PN532 Product Datasheet	115430.pdf
3	NFC Transmission Module Antenna and RF Design Guide	100720.pdf
4	DESfire cards specification	M075031.pdf
5	Mifare cards specification	http://www.nxp.com/products/identification/datasheets/
6	ISO/IEC 14443 specification (T=CL)	ISO/IEC 14443-3 specification ISO/IEC 14443-4 specification
7	NFCIP-1 specification	ISO/IEC 18092 or ECMA340 specification
8	PN532C104 application note AN10449_1	133910.pdf

Glossary

NFC	Near Field Communication
HSU	High Speed UART
SMX	Philips SmartMX (Memory Extension)
PCR	Power, Clock and Reset controller
SAM	Secure Access Module
MINT	Multiple Interfaces
PMU	Power Management Unit
DEP	Data Exchange Protocol. (see reference 7)

Pin correspondence: In the documents the following correspondence can be used in the names of the pins:

PN532 Datasheet name (C104 or C106)	Application Note name (C104 or C106)
P70_IRQ	IRQ
P32_INT0	H_REQ
P50_SCL	SCL
HSU_RX	T_RX
HSU_TX	T_TX

IC correspondence: In the documents the following correspondence can be used in the names of the IC:

Commercial Name	Application Note name
PN5321A3HN/C106	PN532C106
P5CN072	SMX

2. Hardware changes compared to PN532C104

2.1 Hardware configuration pins

At start up, the normal mode must be selected by connecting P35 and IRQ as defined below. The two other modes (RF field on and Emu Joiner) are special modes useful only for tests purposes.

No external resistors are required on P35 and IRQ pins.

	Interface Selection Pin	
	P35 (pin #19)	**IRQ** (pin #25)
Normal mode	1 DVDD/VBAT	1 PVDD
Normal mode	1 DVDD/VBAT	0 GND
EmuJoiner	0 GND	1 PVDD
RF field On	0 GND	0 GND

Three interfaces are available: I2C, SPI and HSU (high speed UART). The interface is selectable by hardware (pin I0 and I1).

	Interface Selection Pin	
	I0 (pin #16)	**I1** (pin #17)
HSU	0 GND	0 GND
I2C	1 DVDD	0 GND
SPI	0 GND	1 DVDD

The embedded software manages the communication with the host controller (I2C, SPI, or HSU interface, protocol on the host link) and the communication on the RF side.

2.1.1 Additional lines (IRQ and H_REQ)

P31 is **not** used to choose between handshake or standard mode: PN532C106 implements **only handshake mode**, whatever P31 configuration (It can be let not connected).

2.1.2 SPI

Only SPI mode 0 is implemented in PN532C106. Consequently, P30 (pin 24) and P33 (pin 33) states don't configure anymore the SPI mode. They can be let not connected

To stay in LowVbat mode, NSS must be kept in high state even when PVDD is not present (NSS low is a wake up condition).

2.2 Host link protocol

No changes compared to PN532C104. Refer to [1] and [8]

2.3 Typical application diagrams

2.3.1 I2C application diagram

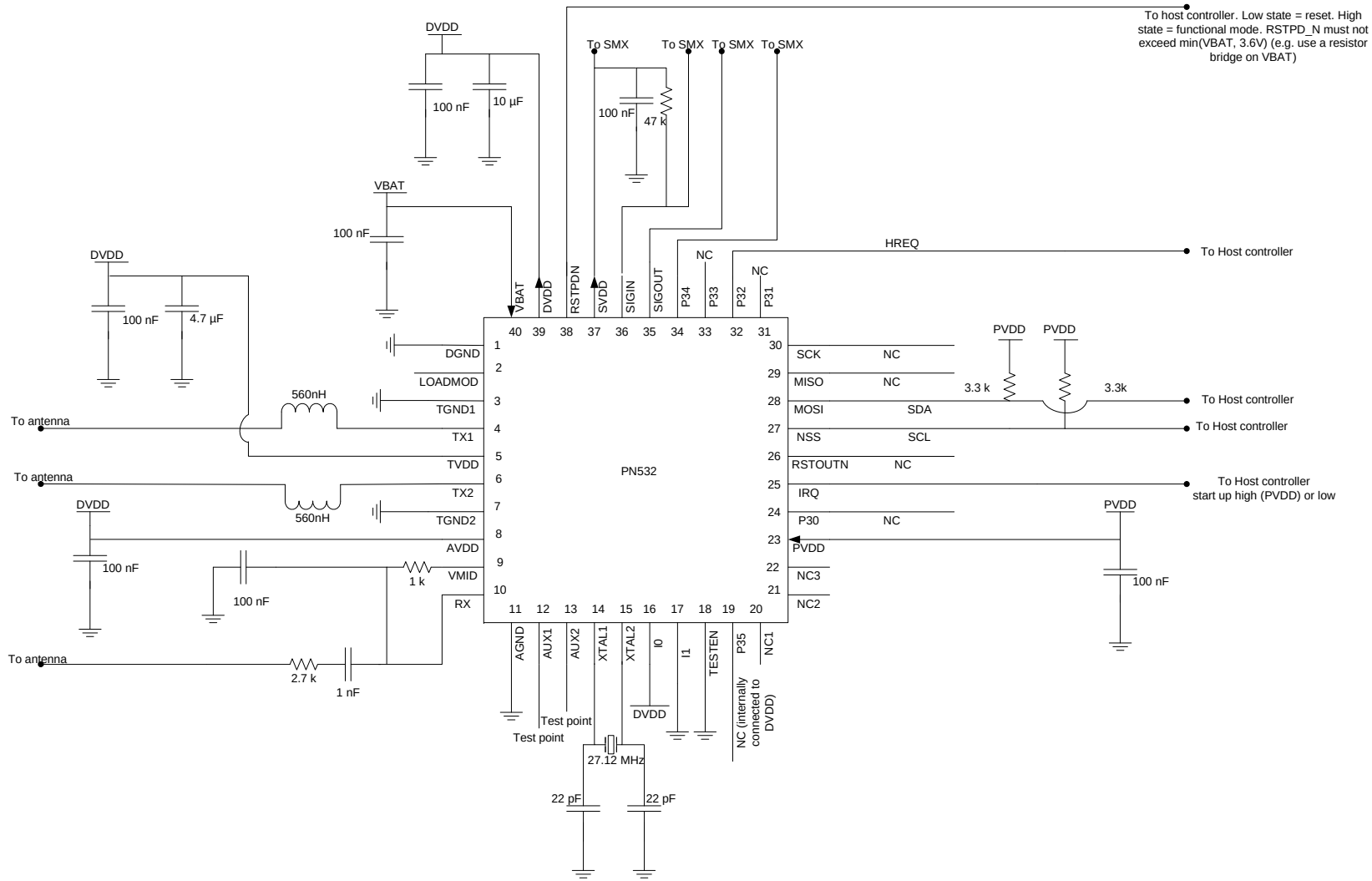


Fig 1. I2C PN532C106 application diagram

2.3.2 SPI application diagram

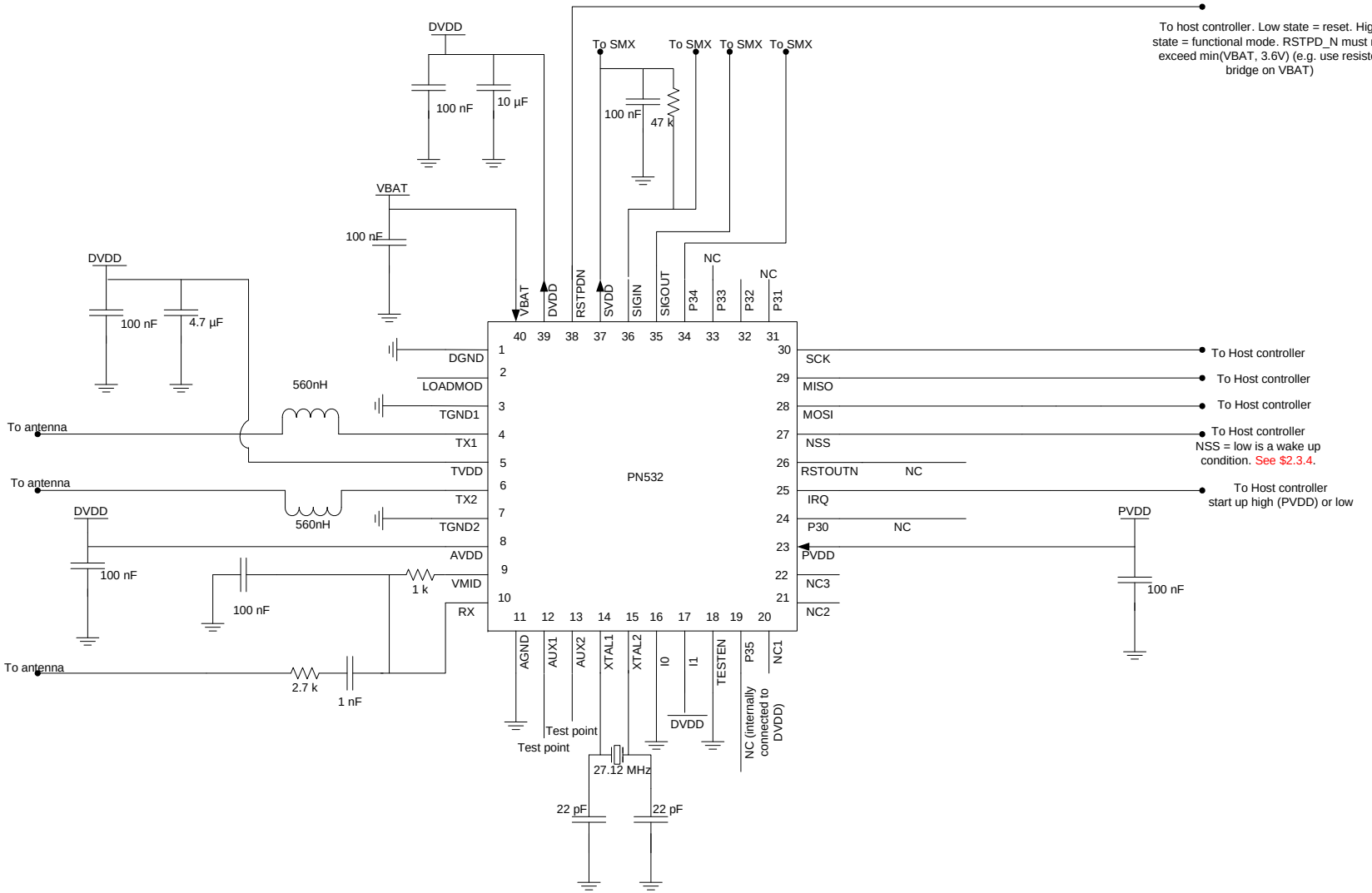


Fig 2. SPI PN532C106 application diagram

2.3.3 HSU application diagram

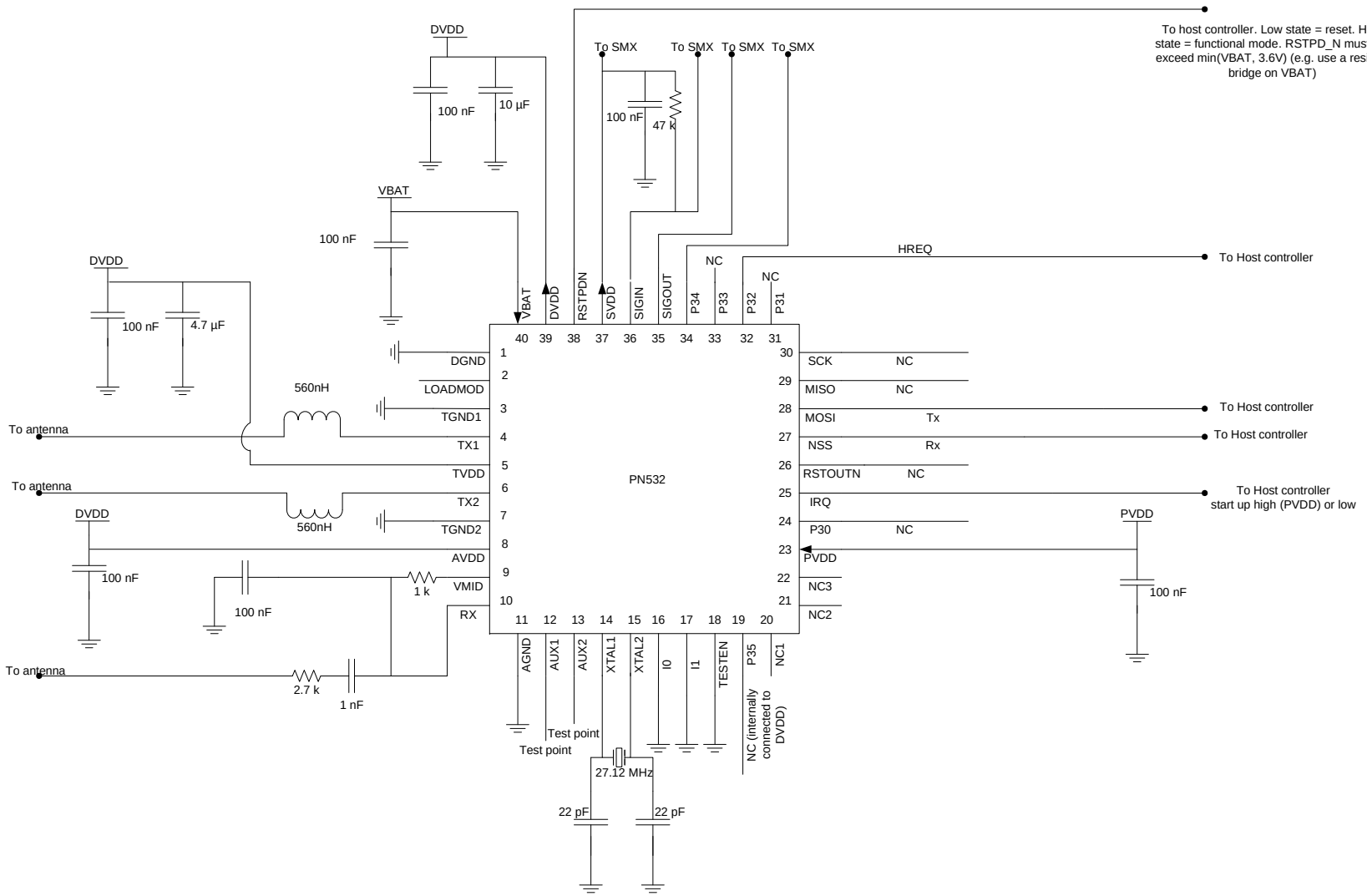


Fig 3. HSU PN532C106 application diagram

2.3.4 Default pin configuration

Consequently, the default pin configuration is as described in the PN532 datasheet. (The default pin configuration is not changed by the PN532C106 firmware).

Pin	Configuration	Additional information
I0 I1	Input	Connect directly to DVDD or to GND (no need of external resistor)
PVDD	Power pin	Externally supplied regulated voltage, 1.6V to 3.6V
RSTPD_N	Input	NFC reset signal. (Low state = reset) RSTPD_N must never exceed min(3.6 V, VBAT)
P30 / UART_RX P31 / UART_TX P32_INT0 P33_INT1 P34 / SIC_CLK P35	Quasi bi directional	No need of external resistor. When connected to the P5CN072, to be used in Virtual Card mode, P34 / SIC_CLK shall be connected to P5CN072 I02
P70_IRQ	Quasi bi directional	No need of external resistor. In the Application Note P70_IRQ will be written as IRQ when used as interrupt line.
MISO / P71	In I2C mode: Quasi bi directional	No need of external resistor.
	In SPI: Push pull	No need of external resistor
	In HSU: Quasi bi directional	No need of external resistor
SCK / P72	In I2C mode: Quasi bi directional	No need of external resistor.
	In SPI: Input	No need of external resistor.
	In HSU: Quasi bi directional	No need of external resistor
MOSI / SDA / HSU_TX	In I2C mode: Open drain	Use pull up, 1k/V. E.g. for PVDD = 3.3V, 3.3 k pull-up.
	In SPI: Input	No need of external resistor
	In HSU: Push pull	No need of external resistor
NSS / P50_SCL / HSU_RX	In I2C mode: Open drain	Use pull up, 1k/V. E.g. for PVDD = 3.3V, 3.3 k pull-up.
	In SPI: Input	Use resistor bridge or LDO and pull up to be able • to keep NSS high even when PVDD = 0 (to stay in LowV_{BAT} mode) • to force a low state to wake up.
	In HSU: Input	No need of external resistor

2.4 How to start the PN532C106?

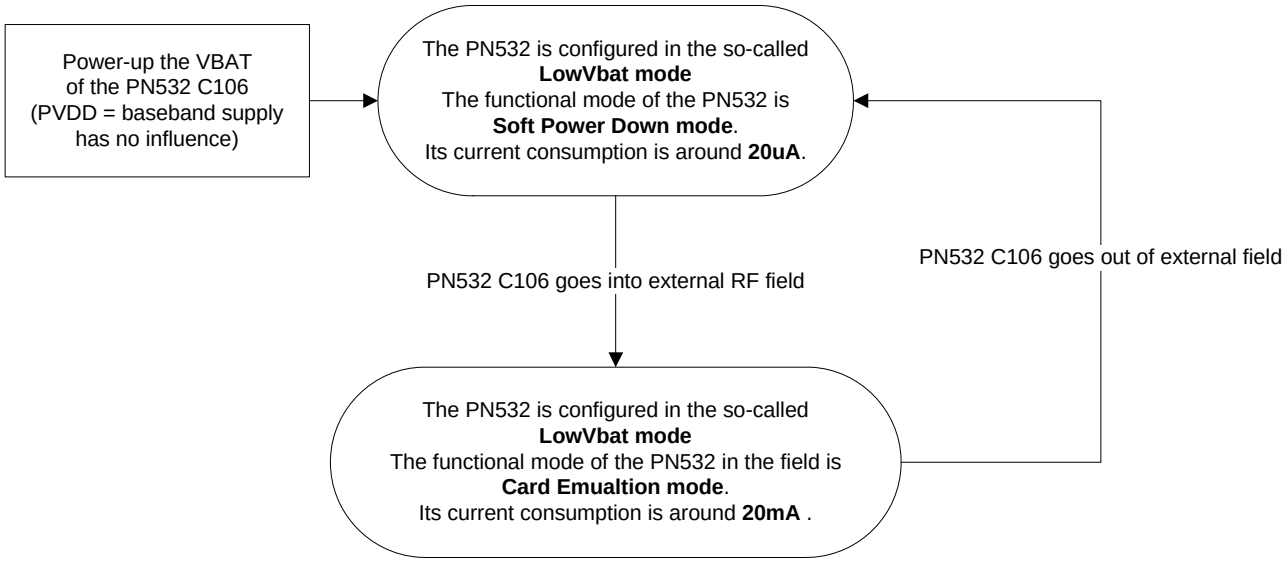
2.4.1 PN532C106 start up default mode : “Low Vbat” mode.

PN532C106 starts in “Low Vbat” mode.
In this mode, the PN532C106 is in virtual card mode when an external field is present, and in power down mode otherwise. In this mode, an external reader can communicate with the SMX (connected to PN532C106 via its S2C interface).

- **No interrupt (IRQ) will be returned by PN532C106 to its host controller.**
- **The host controller cannot wake up PN532 using HREQ/P32 line (pin 32).**

This mode is functional even if PVDD = 0V. (V_{BAT} between 2.7V and 5.5V)

LowV_{BAT} diagram and power consumption:



2.4.2 To go out Low Vbat mode (i.e. to wake up PN532C106 after start up)

To go out “Low Vbat” mode, there are three conditions

- PVDD must be present.
- Moreover, to wake up the PN532**C106**, the host controller must
  - In I2C

  Send PN532 I2C address (48h). The PN532 will stretch low the SCL line during 1 ms (can be less depending on the quartz). The host controller shall wait for the end of the stretching.
  - In SPI

  Set NSS low during 1 ms (can be less depending on the quartz)
  - In HSU

  Send a preamble 55 55 00 00 00 00 00 FF then Len LCS ….

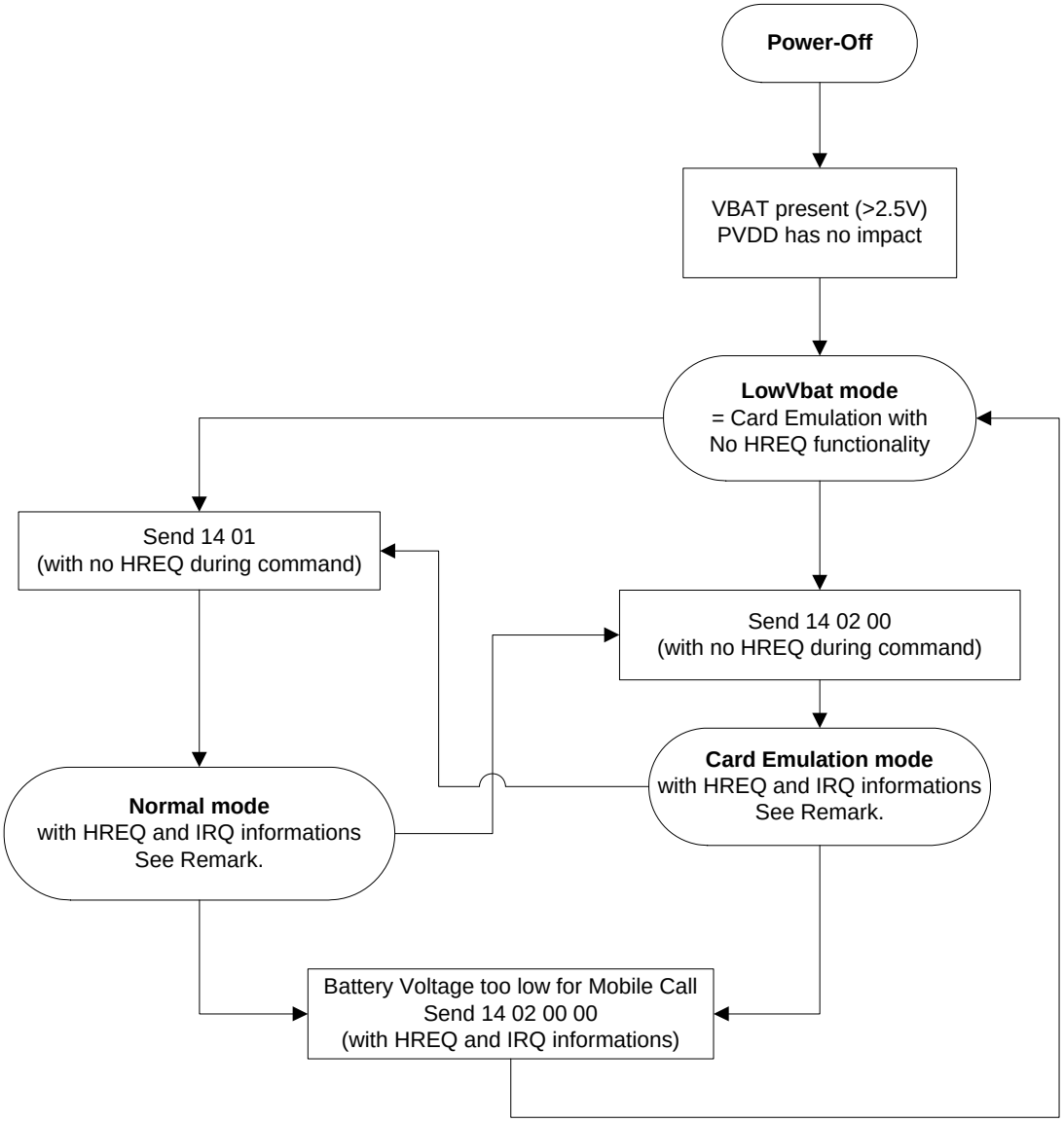
- The host controller must send one of the following commands (using the wake up conditions described just above)
  - Either it wants to stay in virtual card mode. Then it shall send a command to enable the interrupt generation (IRQ) by PN532**C106**. (The IRQ warns the host controller that a transaction occurred between an external reader and the SMX).

  The command to send is “SAM Configuration” with parameter Mode = virtual (02h) and parameter IRQ use = yes (either put value 01h or omit the parameter).
  So the command is ‘**14 02 00**’ (or ‘14 02 00 01’)
  - Or it wants to go to normal mode. Then it shall send “SAM Configuration” with parameter Mode = normal (01h). So the command is ‘**14 01**’

  Once woken up, any command can be send like in PN532C104 (with handshake mode)

  NB: As soon as PVDD is present, the host controller must send a command to enable the interrupt generation (IRQ) by PN532C106**. (The IRQ warns the host controller that a transaction occurred between an external reader and the SMX).** The command to send is “SAM Configuration” with parameter Mode = virtual (02h) and parameter IRQ use = yes (either put value 01h or omit the parameter)
  14 02 00 (or 14 02 00 01)

Instructions described in this paragraph are represented on the following diagram:



Remark: In that modes, in order to fullfill the application requirements, any commands of the User Manual can be sent using HREQ and IRQ informations. These scenarios are not described in the diagram.

3. The PN532 commands

PN532C106 commands are described in reference [1]. Same operating modes (initiator, target, reader, …) than PN532C104 can be used (see reference [8]).

The commands changes are described below.

3.1 Innovision Topaz card reader

In addition to commands described in reference [8], InDataExchange with parameter 0x10 RSEG (Read Segment), is implemented.

Topaz/Jewel command code	Command description
0x00	Read all bytes
0x01	Read a single byte
0x1A	Write-no-Erase a single byte
0x1C	Write-no-Erase 8 bytes
0x53	Write-with-Erase a single byte
0x55	Write-with-Erase 8 bytes
0X10	**Read Segment**

3.2 Frame Delay time

Default The frame delay time (FDT) value changed between PN532C104 and PN532C106

DELAY_MF_SO hardware default value is 0. But in PN532C104, the embedded software sets DELAY_MF_SO to 1 (when command SAMConfiguration is sent).

In PN532C106, the embedded software doesn't change DELAY_MF_SO (so its value is 0)

Address of the register: bit 5 of register address 0x630D. (DELAY_MF_SO bit of Manual Rcv register. See reference 2). To change the value a WriteRegister command can be used, after SAMconfiguration.

3.3 Virtual card mode with no IRQ

When PN532C106 is configured by the host controller with SAMConfiguration command in virtual card mode without IRQ (Command 1”4 02 00 00” : i.e. no IRQ will be generated by PN532), the H_REQ line cannot be used by the host controller to wake up the PN532.

(The chip behaves like in Low Vbat mode, as described in paragraph 2.4)

3.4 InAutopoll

It is possible to poll for two FeliCa cards in the field with PN532C106 (not possible with PN532C104).

4. Recommendations/ known limitations

- **It is not possible to use an external clock with the PN532**
- **FeliCA SIC is not working properly in Wired mode as there is a missing connection between SIGIN and the digital PLL in that mode.**
- **Metachaining in case of bad RF condition (RF error handling)**

  It is recommended not to use Metachaining functionality without a frame integrity check mechanism implemented at the host side, because the PN532 can lose some bytes, in case RF conditions are bad (this happens only in case of RF communication problems)

  DEP Metachaining on the target side:
  When the tox-req is not seen over the air by the initiator on the last packet in a metachained frame, the last packet erases the previous one in the response of the command TgGetData.

  DEP Metachaining on the initiator side:

  The repetition of a frame, in case of non-receiving ACK, does not concatenate the remaining bytes of a previous InDataExchange command

  The host controller (of both target and initiator) must implement a frame integrity check mechanism, or shall use chaining mechanism only.

- **Echo Back Test in 106 kbps on the target side:**
  The Diagnose command (NumTst = 0x05) is not functional the first time it is launched.

  Workaround: The host controller shall send the command TgInitAsTarget before launching the Diagnose command (NumTst = 0x05) in 106 kbps

- **ISO/IEC 14443-4A PICC emulation: R(ACK) resent after R(NACK) reception (RF error handling)**
  Just after reset, in a chained frame, the R(ACK) is resent when a R(NACK) has been received. In a second chained frame, the R(ACK) (with wrong block number) is resent with some other data (the last TgSetData length) when a R(NACK) has been received.

  The host should reset the the PN532 acting as PICC by sending a soft reset (writing 0x01 in the ControlRegister at address 0x6203)

- **PN532 as Initator and PN512 as Target**

  DEP Metachaining on Initiator side: The number of remaining byte is not reset

  If the last frame sent on the RF side is a concatenation of the last frame and the remaining bytes of the previous frame on the host side, the number x of remaining bytes is not reset. As a consequence, the last x bytes of the next RF frame are sent twice

  The host shall reset the number of remaining bytes when Metachaining is finished (writing 0x00 at address 0x01E4)

- **PN532 as Initator and PN531 as Target**

  Peer to peer exchange: the target is taken away from the initiator and is put quickly back

  when a PN531 configured as target is taken away from a PN532 configured as initiator during a peer to peer exchange in Active mode, it may happen that the PN531 does not respond an Attention response to an Attention request.

  Instead, it begins a DEP exchange with MI bit set. So far, where the data within the DEP exchange frame come from needs further investigation.

  In addition, the PN532, receiving an INF pdu as response to an Attention request, does not stop the exchange. Instead, it sends an ACK to the target; so, the target continue its DEP exchange.

5. Annex: pictures of scenarios, with I2C interface

5.1 Introduction

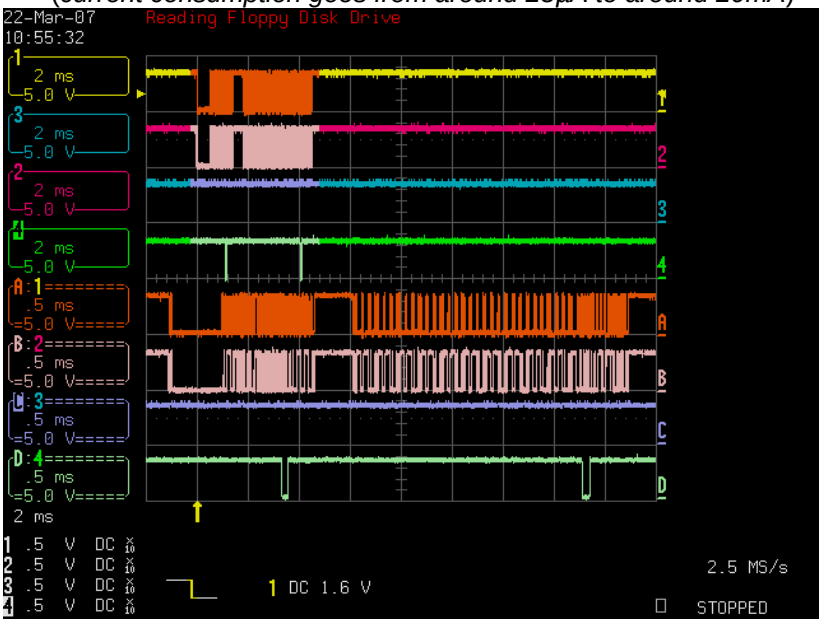
In the following scope pictures the channels are:

1- SCL
2- SDA
3- P32_INT0 (H_REQ)
4- P70_IRQ (IRQ)

5.2 Initialization sequence to use the Normal modes (R/W, P2P…)

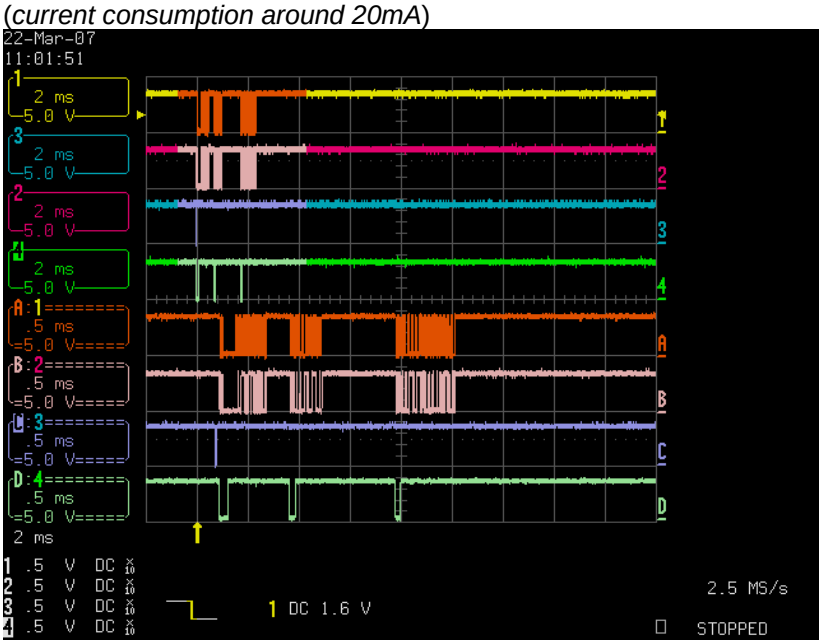
These are the cases using the SAM config command 14 01…

1. Command 14 01 sent to the PN532: The PN532 stretches the SCL line until woken up.
   IRQ is asserted when ACK and answer frames are ready.
   (*current consumption goes from around 25µA to around 20mA*)



2. Now, the PN532 is in normal mode (same as default mode for C104).
   The picture shows an example of command 02 (GetFirmwareVersion) sent to the PN532: H_REQ is used, but is optional (Fig. 39 and 40 of user manual).
   IRQ is asserted when ACK and answer frames are ready.

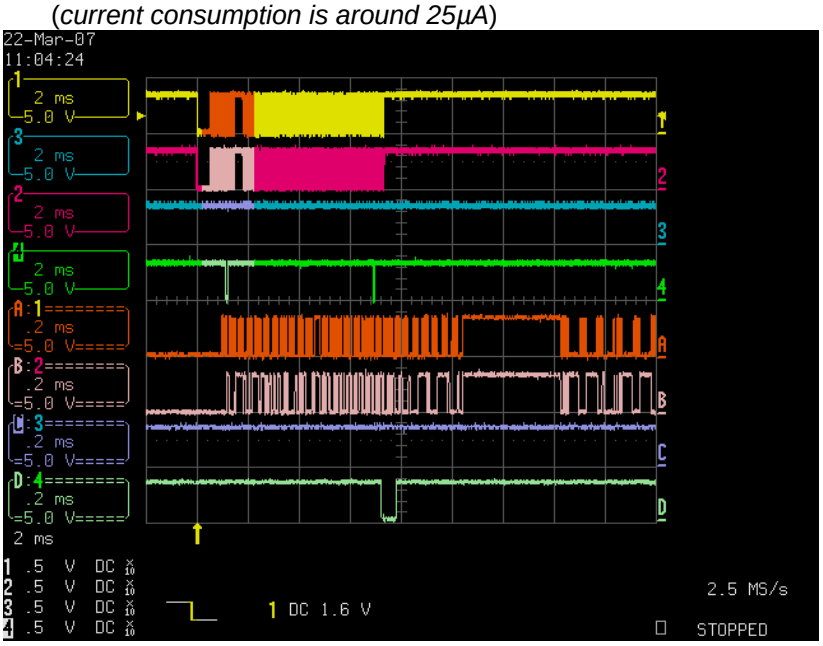
(*current consumption around 20mA*)



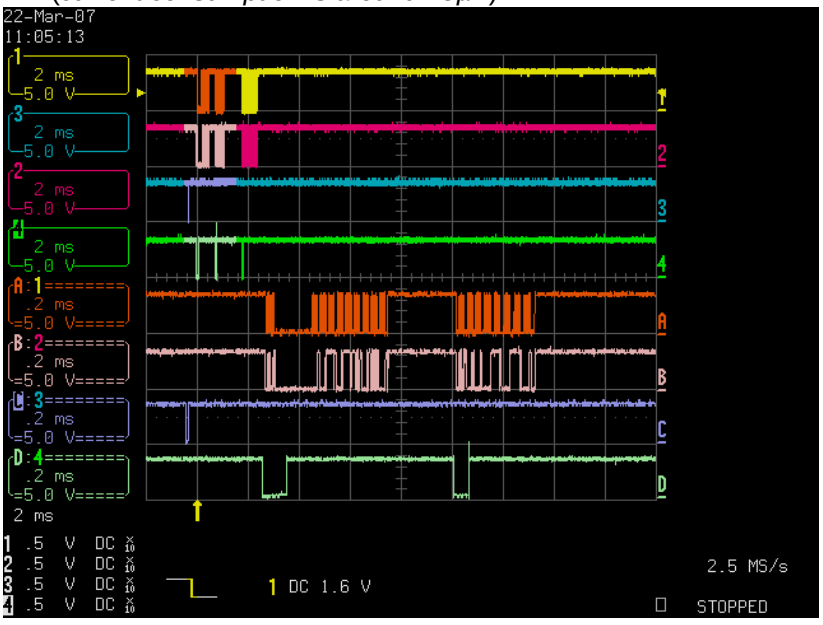
5.3 Initialization sequence to use the Card Emulation Mode with IRQ information available

This the case using the SAM config command: 14 02 00.

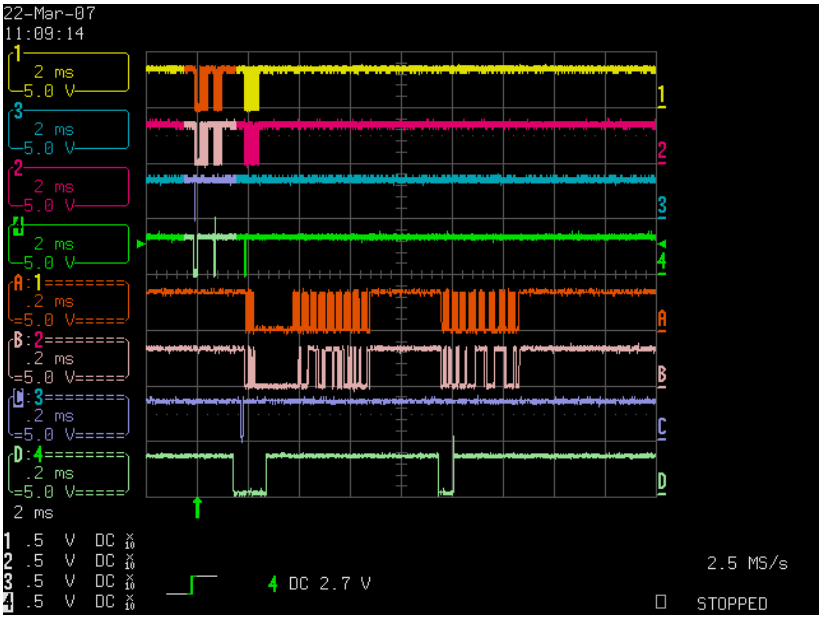
1. Command 14 02 00 is sent to the PN532: The PN532 stretches the SCL line until woken up.
   IRQ is asserted when ACK and answer frames are ready.
   (*current consumption is around 25µA*)



2. Now, the PN532 is in card emulation mode.
   The picture shows an example of command 02 (GetFirmwareVersion) sent to the PN532: H_REQ is used, but is optional (Fig. 41 and 42 of user manual).
   IRQ is asserted when ACK and answer frames are ready.
   (*current consumption is around 25µA*)



3. An external R/W does a contactless transaction, the PN532 informs the host controller of this transaction.
   The picture shows that once the RF transaction completion is detected, the PN532 asserts the IRQ line to inform the host controller.
   (*current consumption is around 25µA if out of external RF field, around 20mA if located in an external RF field*)



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